REMARKS

This is a response to the Final Office Action dated January 6, 2005. Claims 1-41 are pending in the application. In the Office Action, the Examiner rejected Claims 1-23 under 35 U.S.C. §112, first paragraph for not enabling one of ordinary skill in the art to make and use the invention. In addition, Claims 1-41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,392,654 to Gallotta et al. ("Gallotta et al.") in view of U.S. Patent No. 4,744,078 to George P. Kowalczyk ("Kowalczyk"). With this response, claims 1, 11, and 24 have been amended, claims 8, 18, and 31 have been canceled, and claims 42-45 have been added.

The rejections from the Office Action of January 27, 2006 are discussed below in connection with the various claims. No new matter has been added. Reconsideration of the application is respectfully requested in light of the following remarks.

I. REJECTIONS UNDER 35 U.S.C. § 112, first paragraph

Independent claims 1 and 11 were rejected under 35 U.S.C. § 112, first paragraph as not enabling one of ordinary skill in the art to make and use the invention. Applicants submit that the specification does enable one of ordinary skill in the art to make and use the invention of claims 1 and 11, as amended, and respectfully request that these rejections of these claims be withdrawn. Similarly, dependent claims 2-10 and 12-23 were rejected under 35 U.S.C. § 112, first paragraph as not enabling one of ordinary skill in the art to make and use the invention. Dependent claims 2-10 and 12-23 depend from claims 1 and 11, respectively, and should be allowed for at least the reasons set forth for the independent claims. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

II. REJECTIONS UNDER 35 U.S.C. § 103(a)

Independent claims 1, 11, 24, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gallotta et al. in view of Kowalczyk. Applicants submit that claims 6-7, 16, 17, 29, 30 and 37-38 are patentable over Gallotta et al. in view of Kowalczyk because these references, alone or in combination, fail to teach or suggest all of the elements of these claims.

Independent claim 1, as amended, relates to a "packet processing system." The system includes: "a processor; a co-processor separated from said processor by a boundary; and an interface coupled with said processor and said co-processor and operative to bridge said boundary , said interface including: a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and control logic coupled with said at least two read/write ports; wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory; said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory; and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor by detecting when said co-processor has stored data to said memory and signaling said processor of the detected store and by detecting when said processor has stored data to said memory and signaling said co-processor of the detected store; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Independent claim 11, as amended, relates to an "interface for coupling a processor to a co-processor across a boundary, said processor and said co-processor being separated by said boundary." The interface includes: "a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and control logic coupled with said at least two read/write ports; wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory; said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory; and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor by detecting when said co-processor has stored data to said memory and signaling said processor of the detected store and by detecting when said processor has stored data to said memory and signaling said co-processor of the detected store; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Independent claim 24, as amended, relates to a "method of interfacing a processor with a co-processor across a boundary, said processor and said co-processor being separated by said boundary." The method includes: "(a) receiving first data from said processor via a first interface; (b) storing said first data in a memory; (c) detecting, by control logic, that said first data is intended for said co-processor; (d) signaling, by said control logic, said co-processor that said first data has been stored; (e) receiving a read command from said co-processor via a second interface; and (f) providing said first data to said co-processor via said second interface across said boundary; wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Independent claim 34 relates to an "apparatus for facilitating communications between a first processor and a second processor." The apparatus includes: "a dual port memory coupled with said first processor via first interface and said second processors via a second interface, and operative to act as a message buffer between said first processor and said second processor; control logic coupled with said dual ported memory and operative to detect communications by one of said first and second processors and inform the other of said first and second processors of said communications; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Gallotta et al. discloses, "A method and apparatus for processing data with improved concurrency that begins when a host processor an application identifies a memory block of a plurality of memory blocks based on memory block status. The application then provides a data block to the memory block. The data block includes data for processing, which includes application data and operating instructions, and a memory block status update command. A data retrieval command and a sequential updating command are provided to a processing entity by the application. The processing entity then retrieves the data block in accordance with the data retrieval command and processes the memory block status update command to produce an updated memory block status. Finally, the processing entity provides the updated memory block status to the application in accordance with the sequential updating command." *See* Gallotta et al., Abstract.

Kowalczyk discloses, "A data transfer controller allows data to be transferred from a network bus to a system bus in a host computer. The controller has a network bus interface for communicating with the network bus and a system bus interface for communicating with the

system bus. The system bus interface has first and second buffers. A dual port memory is utilized and has one port operatively connected to one of the buffers in the system bus interface and to a microprocessor. The direct access channel is established and operatively connected to the other buffer of the system bus interface as well as coupled to the microprocessor and associated control logic. A switch under control of the control logic establishes connections between the second port of the dual port memory and either the direct access channel or the network bus interface." *See* Kowalczyk, Abstract.

Applicants submit that the combination of Gallotta and Kowalczyk fail to disclose at least control logic "operative to detect when said co-processor has stored data to said memory and to signal said processor [of the detected operation]," as claimed. The system of Gallotta et al. includes a processor which writes data to a memory and causes a co-processor to read the data. After reading the data, the co-processor advances a pointer to an address in the memory which is then used by the processor for the next write operation. Thus, the processor and co-processor in the system of Gallotta et al. communicate directly instead of using the claimed control logic.

Kowalczyk fails to fill the gap. Kowalczyk discloses a system in which data is transferred between a system bus (i.e. first processing entity) and a network bus (i.e. second processing entity). A microprocessor and control logic manage the data transfer. The transfer is managed using a switch that operatively connects either the system bus or the network bus to a single port of a dual ported memory. Kowalczyk, Abstract. When either the system bus or network bus wishes to transfer data, they must inform the microprocessor and control logic directly, for example, by using interrupts. See, e.g., Kowalczyk, Col. 4, lines 4-10. Accordingly, the system of Kowalczyk teaches away from control logic that detects memory store operations. As neither Gallotta et al. and Kowalczyk each fail to disclose a system that includes control logic "operative to detect when said co-processor has stored data to said memory and to signal said processor [of the detected operation]," the combination of Gallotta et al. and Kowalczyk also fails to disclose this element of these claims.

For at least these reasons, claims 1, 11, 24, and 34 are patentable over the combination of Gallotta et al. and Kowalczyk. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

Dependent claims 2-7, 9-10, 12-17, 19-23, 25-30, 31-33, and 35-42 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Gallotta et al. and

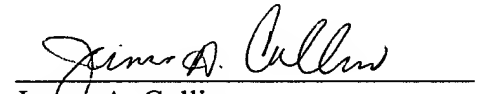
Kowalczyk. Dependent claims 2-7, 9-10, 12-17, 19-23, 25-30, 31-33, and 35-42 should be allowed for the reasons set out above for the independent claims. Applicants therefore request that the Examiner withdraw this rejection of these claims.

SUMMARY

Each of the rejections in the Office Action dated January 27, 2006 has been addressed and no new matter has been added. Applicants submit that all of the pending claims are in condition for allowance and notice to this effect is respectfully requested. The Examiner is invited to call the undersigned if it would expedite the prosecution of this application.

Respectfully submitted,

Dated: April 27, 2006



James A. Collins
Registration No. 43,557
Attorney for Applicants

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200